| | Application No. | Applicant(s) |
|--|--|------------------------|
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| Notice of Allowability | 10/820,128 Examiner | IKEDA ET AL. Art Unit |
| | Cxammer | Artonit |
| <u> </u> | DAVID VU | 2818 |
| The MAILING DATE of this communication appears on the cover sheet with the correspondence address All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308. | | |
| 1. This communication is responsive to <u>04/08/04</u> . | | |
| 2. The allowed claim(s) is/are <u>26-35</u> . | | |
| 3. The drawings filed on <u>08 April 2004</u> are accepted by the Examiner. | | |
| 4. | | |
| Attachment(s) 1. ☑ Notice of References Cited (PTO-892) 2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948) 3. ☑ Information Disclosure Statements (PTO-1449 or PTO/SB/O Paper No./Mail Date 04/08/04 4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material | 6. ☐ Interview Summary Paper No./Mail Da 08), 7. ☐ Examiner's Amendr | te |
| | | MCHAFLTFAN |

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DETAILED ACTION

Reason for allowance

The following is an examiner's statement of reason for allowance: None of the references of record teaches or suggests a method for manufacturing a semiconductor integrated circuit device including a memory cell of an SRAM having a first p-channel MISFET and a first n-channel MISFET, and a peripheral circuit having a second p-channel MISFET and a second n-channel MISFET, comprising: selectively introducing a third impurity into first p-channel MISFET forming region by using a mask covering second p-channel MISFET forming region for controlling a threshold voltage such that a threshold voltage of first p-channel MISFET is higher than a threshold voltage of second p-channel MISFET.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance".

Conclusion

2. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Vu whose telephone number is 571-272-1798. The examiner can normally be reached on Monday-Friday 8:00am-5:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's

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supervisor, David Nelms can be reached on 571-272-1787. The fax phone numbers for the

organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR, Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PV

David Vu.

December 21, 2004.

MICHAELTRAN PRIMARY EXAMMER